Amendments to the Specification

Please replace paragraph on page 11, lines 10-12 with the following amended paragraph:

A1

Figs. 3A-3C illustrate ~~Fig. 3 illustrates~~ a detailed diagram of a first embodiment of a pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention;

Please replace paragraph on page 11, lines 13-15 with the following amended paragraph:

A2

Figs. 4A-4C illustrate ~~Fig. 4 illustrates~~ a detailed diagram of a second embodiment of the pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention;

Please replace paragraph on page 12, lines 1-3 with the following amended paragraph:

A3

Figs. 7A-7C illustrate ~~Fig. 7 illustrates~~ a detailed diagram of a third embodiment of the pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention; and

Please replace paragraph on page 16, lines 11-18 with the following amended paragraph:

A4

Figs. 3A-3C illustrate ~~Fig. 3 illustrates~~ a detailed diagram of a first embodiment of a pseudo-noise encoded digital data clock recovery circuit 300 in accordance with the principles of the present invention. In this embodiment, the pseudo-noise encoded digital data clock recovery circuit 300 correlates the received chip stream with a reference pseudo-noise sequence to generate a correlator output 307. The correlator output 307 is then compared to an upper threshold 310 and a lower threshold 315, and the resulting signals from the upper and lower thresholds are ORed together at a OR gate 320. The OR gate 320 generates a thresholded correlator output signal 321.

Please replace paragraph on page 18, lines 1-8 with the following amended paragraph:

A5 Cont

In systems with multiple samples per chip (referred to as "oversampled") which will be described in details in ~~Fig. 4~~ Figs. 4A-4C, the clock recovery circuit looks for a series of consecutive samples in one bit period to see whether the corresponding counter values exceed a threshold and decide whether the phase shift of the bit clock, is needed. If a counter exceeds the threshold outside the range of counters associated

A5 cont'd

with the chip position of the current bit clock, the bit clock is re-aligned at a different sample position, for example, advancing one sample position or retarding one sample position. If no counters exceed the threshold, the bit clock still remains at the same sample position.

Please replace paragraph on page 18, lines 9-19 with the following amended paragraph:

A6

In systems with oversampled chip streams, the correlator output histogram can be efficiently realized by implementing counters (e.g. the counters 460 through 465) for only a subset of the total sample positions of a bit period. This subset consists of a cluster of consecutive samples spanning an interval, or "window", slightly larger than one chip period. The alignment of this window, relative to the correlator output, is initially set by a reacquisition circuit (e.g. a reacquisition circuit 451 as shown in Figs. 4A-4C ~~Fig. 4~~) based on a preliminary estimate of the most likely position of the corrector bit clock. Preferably, the alignment of this window is such that there is a margin of at least one sample position on either side of the chip period associated with the bit clock. Also, after N bit periods, the counters, such as the counters 360-374, and the registers, such as the register 397, are reset, and the histogram process starts again.

Please replace paragraph on page 18, line 20 to page 19, line 9 with the following amended paragraph:

A7

Figs. 4A-4C illustrate ~~Fig. 4 illustrates~~ a detailed diagram of a second embodiment of the pseudo-noise encoded digital data clock recovery circuit 400 in accordance with the principles of the present invention. As shown in ~~Fig. 4~~ Figs. 4A-4C, fewer counters are used in comparison to the counters used in the embodiment shown in ~~Fig. 3~~ Figs. 3A-3C. For illustrated purposes, six counters 460-465 are used to histogram over a window of consecutive sample positions (e.g. 6 samples) which spans a subset of the total sample positions within a bit period (e.g. 60 sample positions). A window of consecutive sample positions is chosen to be larger than the bit period of one chip while a margin of one sample is at the either side of the chip period. A correlator output 407 from a correlator 405 in a correlation circuit 402 is compared to an upper threshold 410 and a lower threshold 415. The resulting signals are ORed together at a OR gate 420.

Please replace paragraph on page 19, line 18 to page 20, line 11 with the following amended paragraph:

A8 cont

As shown in ~~Fig. 4~~ Figs. 4A-4C, a system may employ four samples per chip and implement a six-sample histogram window. In such a system, one would expect to see spikes at the correlator output 407 most often during the four consecutive sample positions when the bit period of

the incoming chip stream 401 is aligned with the reference pseudo-noise sequence 406 in the correlator 405. During the initial acquisition of the bit clock from the received chip stream 401, the histogram window can be initially placed so as to bracket the four sample positions where 'true' correlator output spikes are expected. The correlator output spikes represent the alignment of the bit period in the received chip stream 401 with the reference pseudo-noise sequence 406. This initial placement of the window may be based on some quick means of guessing where the true correlator output spikes are expected. Using this example, one way of initially placing the window would be to center the window around the first three or four consecutive correlator output spikes observed at the correlator output 407. After this initial placement, the correlator output 407 is histogrammed for N bit periods for those sample positions that fall within the window.

A8 cont

Please replace paragraph on page 23, line 18 to page 24, line 4 with the following amended paragraph:

Figs. 7A-7C illustrate ~~Fig. 7 illustrates~~ a detailed diagram of a third embodiment of the pseudo-noise encoded digital data clock recovery circuit 700 in accordance with the principles of the present invention. The example shown implements four (4) samples per chip and a histogram window size of seven (7) samples. In systems with multiple samples per chip, the phase of a bit clock can be more accurately tracked by calculating the average sample position after each pass through a histogram window. The average sample position is the sum of the histogram accumulator values weighted by their associated sample positions divided by the sum of the histogram accumulator values weighted by one.

A9 cont

Please replace paragraph on page 24, lines 8-11 with the following amended paragraph:

As shown in ~~Fig. 7~~ Figs. 7A-7C, a ΔCOR 710 in a correlation circuit 703 is the absolute value 708 of 7.5 (1/2 of 15) 704 minus a COR 702 rounded down to the nearest whole number 706. The ΔCOR 710 then passes through the seven low pass filter (LPF) counter/accumulator 720–732 as shown in Fig. 6.

A10

Please replace paragraph on page 25, lines 14-19 with the following amended paragraph:

A decoder 715 in the location circuit 714 is used to enable the integration of the correlator output at each sample position. The decoder 715 is controlled by the output of the counter 788. If the accumulators 720 through 732 fail to register sufficient counts to indicate alignment of

A11 cont

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the correct bit clock with the histogram window, a reacquisition can be performed by a reacquisition circuit 791 by reacquisition circuitry components 790–798, similar to the reacquisition circuit components 452-458 shown in ~~Fig. 4~~ Figs. 4A-4C.